OZ711 SCR REGISTER DESCRIPTIONS

Address	Register	Function	Use	Read/ Write	Size (bytes)
00 0000	MANUAL_E_R	Bi-directional signal lines are Receiver or Emitter	Synchronous cards	R/W	1
00 0010	FRQ_MODE	Frequency division rate choice		R/W	1
00 0100	MODE	Functional options choice		R/W	1
00 0110	CARD_MODE	Smart card modes and GIC parameters			
00 1000	PROTO	Protocol used and its parameters		R/W	1
00 1010	ETU_INI	Card reset ETU		R/W	2
00 1100	ETU_WRK	Working ETU		R/W	2
00 1110	CGT	Extra guard-time	T=0, T=1	R/W	1
01 0000 (msb) 01 0010 (lsb)	CWT	Waiting time between bytes	T=0, T=1	R/W	4
01 0100 (msb) 01 0110 (lsb)	BWT	Waiting time between blocks Waiting time for TS byte in ATR	T=1 only	R/W	4
01 1000	CLK_CNT	Clock cycles counter		W	2
01 1010	ETU_CNT	ETU counter		W	2
01 1100	MASK_IT	Interruption mask		R/W	1
01 1110	FIFO_LEV	FIFO level that activates the interrupt IT_REC		R/W	2
10 0000	EXE	Execution of one command of the module		R/W	2
10 0010	STATUS_IT	Status of the interrupts activated by the module		R	1
10 0100	DEVAL_IT	Interrupt acquittal by the micro-controller		W	1
10 0110	STATUS_EXCH	Smart card exchange status		R	2
10 1000	FIFO_NB	Number of bytes received in FIFO		R	2
10 1010	IO_MUTE	Time without activity on IO (Level 1)		R	2

IO Registers:

Address	Register	Function	Use	Read/ Write	Size (bytes)
00 0000	MANUAL_IN	Signals applied to smart card contacts	Synchronous cards	R/W	1
00 0010	MANUAL_OUT	Smart card contacts	Synchronous cards	R	1
00 0100	FIFO_IN	Enter data in FIFO		W	1
00 0110	FIFO_OUT	Read data from FIFO		R	1
00 1000	XOR_REG	Exclusive OR of data received in FIFO		R	1
00 1100 (mob) 00 1110 (lbs.)	CRC16	CRC16 computation of data received in FIFO		R	2
01 0000	MOTO_CFG	Manual configuration		R/W	1

Configuration Registers

The one-byte configuration registers defined below are in fact mapped on two bytes with only the least significant byte (LSB) useful. The most significant byte (MSB) is Reserved for Future Use (RFU).

The Manual mode allows the micro-controller to drive the smart card contacts directly, in case of asynchronous card, for example. This mode requires three registers:

- MANUAL_E/R specifies the bi-directional signal lines as Receiver or Emitter
- MANUAL_IN that the microprocessor writes values to be applied to smart card contacts
- MANUAL_OUT contains the actual smart card contact state.

MANUAL_E_R (R/W)

This register specifies the bi-directional signal lines as Receiver or Transmitter.

Bit	Name	Reset Value	Function
b8	I_O _dir	1	0: IO in transmission mode 1: IO in reception mode (tri-state)
b7	C4 _dir	1	0: C4 in transmission mode 1 : C4 in reception mode (tri-state)
b6	C8 _dir	1	0: C8 in transmission mode 1: C8 in reception mode (tri-state)
b5	rfu	0	
b4	rfu	0	
b3	rfu	0	
b2	rfu	0	
b1	rfu	0	

FRQ_MODE (R/W)

This register programs the frequency options of the module.

Bit	Name	Reset value	Function
b8 b7 b6 b5	DIV_RATE	0011	Clock division rate
	XXXX		The division rate to use divided by two. Examples :
	0001		Division rate is two
	0010		Division rate is four
	1111		Division rate is thirty
	0000		*Warning: 0 is not possible. Instead, the division rate is two.*
b4	CLK_LEV	0	Clock state in sleep mode must be 0: Clock set to 0 1: Clock set to 1
b3	RFU	0	
b2	RFU	0	
b1	RFU	0	

***Notes**: The possible division values include all even numbers from 2 to 30.*

When CRD_ACT=1 in STATUS_EXCH register, if DIV_RATE changes, it will not be taken into account until CRD_ACT = 0.

MODE (R/W)

This register programs the module's functional options.

Bit	Name	Reset Value	Function
b8	CRD_DET	0	When no smart card is inserted, the smart card presence detector indicates: 0: Level 0 1: Level 1
b7	EDC	0	EDC (XOR or CRC16) 0: is calculated by the module from the data in FIFO 1: is written in FIFO by the microprocessor at the end of the block
b6	RFU	0	
b5	ATR_TO	0	Program the waiting time of the answer to reset after activation of CLK or RST. 0: normal waiting time of 40 000tcy 1: the waiting time is indicated in BWT register
b4	MANUAL	0	Manual mode 0: disable 1: enable
b3	RFU	0	
b2	RFU	0	
b1	RFU	0	

Notes: *If the micro doesn't have time to calculate the EDC of the command to send to the smart card, it sets MODE.EDC to 0 (and clears the XOR or CRC16 registers). Then it writes its command in the FIFO, the calculation will be done automatically in those registers. When sending the block to the smart card, the module send the content of XOR or CRC16 after the data in FIFO. Then it clears XOR or CRC16 registers before receiving the smart card answer.*

CRD_DET must be affected before releasing the master reset. If not, its default value is 0.

CRD_DET must not be modified after the release of master reset, unless it may generate unwanted SCI or SCP interruptions. CRD_DET is not taken into account during soft reset. It is recommended to take special care of this bit when setting parameters into MODE register after the master reset.

CARD_MODE (R/W)

This register specifies various smart card modes. It also specifies the chip parameters choice.

Bit	Name	Reset value	Function
b8	AS_SY	0	0: Asynchronous Card (AS) 1: Synchronous Card (SY)
b7	Moto_Sel	0	Indicates whether the reader should be configured manually or automatically. 0: Reader is manually configured through the MOTO_CFG register. 1: Reader is automatically configured by the module.
b6	Moto_Par	0	Functional options 0: Smart card power supply is 3V 1: Smart card power supply is 5V
b5 b1	RFU	00000	

***Note**: For synchronous cards, only PON, POF, and RST are available. For command exchange, the Manual mode must be used. Exch and PTS operations are access-protected.*

PROTO (R/W)

This register indicates which protocol is used and specifies its parameters.

Bit	Name	Reset Value	Function
b8	CP	1	T=0 protocol 0: No parity control, in this case RC=0. 1: Parity control
b7	RC	0	T=0 protocol 0: In case of parity error, there will be no character repetition 1: In case of parity error, the module will ask for character repetition. If a parity error appears twice, the module requests character repetition again. If the parity is still wrong, an Err_Par status is returned.
b6	RC_Dur	0	In case of character repetition, the module sets the IO to 0 during: 0: 1 etu 1: 2 etus
b5	EDC_TYP	0	T=1 protocol 0: EDC is LRC (EXCLUSIVE OR from NAD to last V field byte) on one byte (calculation result in XOR register) 1: EDC is CRC16 on two bytes (calculation result in CRC16 register).
b4 b3 b2 b1	PROT_TYP 0 0 0 0 0 0 0 1 x x x x	0000	Protocol as coded in TDi T=0 T=1 RFU

Parity checking by the module:

Parity is correct when the number of «ONES» including parity is even (data + parity byte). «ONE» depends on the convention mode:

- Direct mode: «ONE» is 5V during one etu.
- Inverse mode: «ONE» is 0V during one etu.

Parity management by the module when T=0:

- CP = RC = 0:
- When transmitting, it will send its next data even if IO is maintained to 0 by the smart card.
- During reception, the wrong byte is stored in FIFO without character repetition.

- CP = 1, RC = 0:
  - When emitting, a smart card asking for repetition will generate an End_Exch int and Err_Par status.
  - When receiving, a parity error also generates an End_Exch int and Err_Par status.
- CP = RC = 1:
  - When transmitting, it repeats the byte up to three times; the fourth request generates an End_Exch int and Err_Par status.
  - When receiving, it requests a correct byte twice; if the error persists, the status becomes End_Exch int and Err_Par.

Parity management by the module in case of T=1:

- RC is forced to 0 in case of T=1.
- CP = 0: A parity error is detected if EDC is not 0.
- CP = 1:
  - Not taken into account when emitting
  - When receiving, if an error occurs, the module stops receiving the data and returns an End_Exch interruption and an Err_Par status.

Parity management by the module in case of PTS:

- RC is not taken into account, but it is not forced to 0, it keeps its value for further exchanges.
- CP is interpreted as same as in T=1.

ETU_INI (R/W)

The number in this register indicates the clock cycle number of one answer to reset etu. It is between 23 to 2048 (in decimal); it is coded on two bytes in hexadecimal.

b8	b7	b6	b5	b4	b3	b2	b1	Frequency coding
x	x	x	x	x	x	x	x	High order byte
x	x	x	x	x	x	x	x	Low order byte

Table 11. ETU_INI (R/W)

The reset value of this register is 372 (174 hex), as it is specified in ISO 7816-3: 1 etu = 372/fi.

b8	b7	b6	b5	b4	b3	b2	b1	Reset value of ETU_INI
0	0	0	0	0	0	0	1	High order byte
0	1	1	1	0	1	0	0	Low order byte

ETU_WRK (R/W)

The number in this register indicates the clock cycle number of one etu in card exchanges (other than answer to reset). It is between 23 to 2048 (in decimal). It is coded on two bytes in hexadecimal.

b8	b7	b6	b5	b4	b3	b2	b1	Frequency coding
x	x	x	x	x	x	x	x	High order byte
x	x	x	x	x	x	x	x	Low order byte

b8	b7	b6	b5	b4	b3	b2	b1	Reset Value of ETU_WRK
0	0	0	0	0	0	0	1	High order byte
0	1	1	1	0	1	0	0	Low order byte

CGT (R/W)

Indicates the Extra Guard Time (EGT) N asked by the smart card before receiving the next character. It is coded as TC1 byte in ATR.

Note: *In T=0, no Extra Guard Time (EGT) is allowed after the last command byte and after the last data byte (ISO_IN). This is designed to avoid overwriting the Procedure byte and/or SW1 SW2 bytes transmitted from the smart card.*

But, in case of ISO_IN, the module must wait for the EGT between the end of the procedure byte and the first bit of data to be sent to the smart card.

In T=1, no EGT is allowed after the bloc's last byte.

b8	b7	b6	b5	b4	b3	b2	b1	N Coding
0	0	0	0	0	0	0	0	No EGT (default and reset value)
1	1	1	1	1	1	1	1	Characters transmitted by the module are coded on 11 etus. The module must be ready to receive a start bit at the 11th etu. In this case, RC = 0; no repetition occurs in the event of a parity error.
x	x	x	x	x	x	x	x	Number of EGT etus requested by the smart card. The module should wait for this number + 12 etus between the two starts bits of the bytes sent.

***Note**: Module-> Smart card: CGT = 255 indicates that the module will send characters coded on 11 etus to the smart card.*

Smart card -> Module: if character repetition option is disabled, the module is ready to receive a new start bit at 10,5 etus from the last start bit. At this time, the smart card sends the bytes. The module does not set the IO to 0 to request character repetition. Consequently, when the IO = 0 after 10,5 etus, it has to be the next start bit's leading edge.

CWT (R/W)

Used in T=0 and T=1.

Indicates the character timeout. When this timeout is reached, the TimeOut Character (TOC) interruption is returned.

Card reset: CWT = 9600 etu

T=0: CWT = 960xDxWI etu

Dmax = 16

Wimax = 255

CWT from 960 to 3 976 800 etus, this corresponds to 407 seconds at 9600 bauds or 34 seconds at 115200 bauds.

T=1: CWT = $(2^{CWI} + 11)$ etu

CWImax = 15, then CWT from 13 to 32779etu

CWT is coded in etu on four bytes, so CWTmax = 4 294 967 295etu.

b8	b7	b6	b5	b4	b3	b2	b1	Coding of CWT
x	x	x	x	x	x	x	x	CWT most significant byte
x	x	x	x	x	x	x	x	
x	x	x	x	x	x	x	x	
x	x	x	x	x	x	x	x	CWT least significant byte

The reset value of this register will be the same as for the ATR, that is, 9600 etus (2580 hex).

b8	b7	b6	b5	b4	b3	b2	b1	CWT Reset Value
0	0	0	0	0	0	0	0	CWT most significant byte
0	0	0	0	0	0	0	0	
0	0	1	0	0	1	0	1	
1	0	0	0	0	0	0	0	CWT least significant byte

BWT (R/W)

This register has two functions: BWT when T=1, and ATR timeout.

ATR timeout: if the option MODE.ATR_T0 is validated, the timeout for ATR on IO which is normally 40 000 tcy is indicated in this register. In this case, the time unit is the clock cycle.

Maximum timeout value: 4 294 967 295 tcy

When T=1:

BWT = Smart card answer block timeout. When this timeout is reached, the TimeOut Block (TOB) interruption is returned.

BWT = $(2^{BWI} \times 0,1)s + 11etu$

BWImin = 1, BWT = 0,2s + 11etu

BWImax = 15, BWT = 3276s

BWT is coded in etus on four bytes. The micro-controller converts this time from seconds to etus.

BWTmax = 4 294 967 295 etus.

b8	b7	b6	b5	b4	b3	b2	b1	BWT/ ATR_TO Coding
x	x	x	x	x	x	x	x	Most significant byte
x	x	x	x	x	x	x	x	
x	x	x	x	x	x	x	x	
x	x	x	x	x	x	x	x	Least significant byte

The reset value for this register is calculated with the default value of BWI = 04, so BWT = 1,6s. At 9600 bauds, 1 etu = 104µs. Consequently BWT = 15 360 etu (3C 00h).

b8	b7	b6	b5	b4	b3	b2	b1	BWT Reset Value
0	0	0	0	0	0	0	0	BWT most significant byte
0	0	0	0	0	0	0	0	
0	0	1	1	1	1	0	0	
0	0	0	0	0	0	0	0	BWT least significant byte

CLK_CNT (W)

Sets this counter to value XX and releases the interrupt CLK_IT once XX clock cycles have occurred.

When set to 0, this counter will not launch any interrupt. The reset value is 0.

b8	b7	b6	b5	b4	b3	b2	b1	Coding of CLK_CNT
x	x	x	x	x	x	x	x	Most significant byte
x	x	x	x	x	x	x	x	Least significant byte

ETU_CNT (W)

Sets this counter to XX value and it will release the interrupt ETU_IT once XX etus have occurred.

When set to 0, this counter will not launch any interrupt. The reset value is 0.

b8	b7	b6	b5	b4	b3	b2	b1	Coding of ETU_CNT
x	x	x	x	x	x	x	x	Most significant byte
x	x	x	x	x	x	x	x	Least significant byte

MASK_IT (R/W)

The validated interruptions are those set to one by the micro-controller.

Bit	Name	Reset Value	Function
b8	SCP_MSK	0	Smart card pulled out
b7	SCI_MSK	0	Smart card insertion
b6	CLK_IT_MSK	0	CLK_CNT clock cycles have occurred since loading of CLK_CNT register
b5	ETU_IT_MSK	0	ETU_CNT etu have occurred since loading of ETU_CNT register
b4	RFU	0	
b3	RFU	0	
b2	IT_REC_MSK	0	Indicates that the number of bytes received in FIFO has reached FIFO_LEV.
b1	END_EXE_MSK	0	Indicates that the operation is ended.

***Notes**: This register enables the interruptions useful for the micro.*

The STATUS_IT register indicates the interruptions activated by the module.

The DEVAL-IT register is used by the micro to acquit the activated interruptions (this is done to prevent a simultaneous writing from the micro and the module in the same register).

The interruption signal provided to the micro-controller will be active when set to level 0.

If interruptions are not allowed, the interrupt signal generated by the IT Controller will not be active, but the STATUS_IT register will nevertheless be affected. The micro-controller can then be aware of what's happening and may acquit the interruptions via DEVAL_IT.

FIFO_LEV (R/W)

Indicates the number of bytes stored by the module in the FIFO before activating the IT_REC interruption. It is coded on 2 bytes (because FIFO is 261 bytes length).

b8	b7	b6	b5	b4	b3	b2	b1	FIFO_LEV
rfu	rfu	rfu	rfu	rfu	rfu	rfu	x	High order byte
x	x	x	x	x	x	x	x	Low order byte

This register will be set to 01 in case of reset soft of the module. It cannot be set to 00 (unless IT_REC will be always active), the minimum value is 01.

b8	b7	b6	b5	b4	b3	b2	b1	Reset Value of FIFO_LEV
rfu	rfu	rfu	rfu	rfu	rfu	rfu	0	High order byte
0	0	0	0	0	0	0	1	Low order byte

EXE (R/W)

Setting one bit of this register to 1 launches the corresponding command execution.

When the module has finished, this bit is cleared to 0.

If more than one bit is set at the same time, no execution is launch and those bits are cleared.

Except S_TOC and RESET, if during one command execution another bit is set to 1, it will not be taken into account and the running command ends normally.

S_TOC_EXE can only be executed if the module is in reception from smart card.

If this bit is set to 1 by the application when no other command is running, the module will return the interruption End_EXE and the status Err_EXE.

If it is set to 1 when another command is running but is not in reception mode, the module will return the interruption End_EXE and the status Err_EXE and the other command will end normally.

The RESET_EXE bit has priority.

MOST SIGNIFICANT BYTE:

Bit	Name	Reset Value	Function
b8	POF_EXE	0	Smart card contacts power off sequence
b7	PON_EXE	0	Smart card power on and reset sequence
b6	RST_EXE	0	Smart card hot reset sequence
b5	EXCH_EXE	0	Send the command stored in FIFO to the smart card and receive its answer
b4	CHG_ETU_EXE	0	Change ETU_INI to ETU_WRK
b3	PTS_EXE	0	Protocol Type Selection sequence
b2	S_TOC_EXE	0	Stop the module waiting for a byte
b1	RESET_EXE	1	Module soft reset

LEAST SIGNIFICANT BYTE:

Bit	Name	Reset Value	Function
b8	CLK_SLEEP_EXE	0	Sets smart card to sleep mode: Clock is stopped at FRQ_MODE.CLK_LEV level.
b7	CLK_WAKE_EXE	0	Awakens the smart card from sleep mode: the clock becomes active again.
b6	RST_FIFO_EXE	0	Resets the FIFO pointers; FIFO is then empty.
b5..b1	RFU	00000	

***Notes**: In order to perform a soft reset on the module, the micro-controller must make a pulse to 1 on the RESET_EXE for at least 1µs. The micro-controller releases this bit to 0.*

When reading this bit, the micro-controller will read:

- RESET_EXE = 1 when the module is in normal mode.

- RESET-EXE = 0 when the module is in reset mode.

When the micro-controller has received the whole expected answer, it stops the wait for the timeout by setting the S_TOC bit. Then the module stops receiving and returns an End-EXE.

STATUS_IT (R)

Indicates the interruption activated by the module (set to 1). To acknowledge one interrupt, the micro-controller must clear the corresponding bit in DEVAL_IT.

Bit	Name	Reset Value	Function
b8	SCP	0	Smart card pulled out
b7	SCI	0	Smart card insertion
b6	CLK_IT	0	CLK_CNT clock cycles have occurred since loading of CLK_CNT register.
b5	ETU_IT	0	ETU_CNT etu have occurred since loading of ETU_CNT register.
b4	rfu	0	
b3	rfu	0	
b2	IT_REC	0	Indicate that the number of bytes received in FIFO has reached FIFO_LEV.
b1	END_EXE	0	Indicate that the operation is ended.

***Note**: If no smart card is inserted when releasing the Master reset of the module, no SCP interruption will be generated. But if a smart card is inserted before releasing the Master reset of the module, this will generate an SCI interrupt.*

DEVAL_IT (W)

The micro-controller clears the interrupt bit it wants to acknowledge. The module clears the corresponding interrupt bit in the STATUS_IT register.

Bit	Name	Reset Value	Function
b8	SCP_CLR_B	0	Smart card pulled out
b7	SCI_CLR_B	0	Smart card insertion
b6	CLK_IT_CLR_B	0	CLK_CNT clock cycles have occurred since loading of CLK_CNT register
b5	ETU_IT_CLR_B	0	ETU_CNT etu have occurred since loading of ETU_CNT register
b4	RFU	0	
b3	RFU	0	
b2	IT_REC_CLR_B	0	Indicate that the number of bytes received in FIFO has reached FIFO_LEV.
b1	END_EXE_CLR_B	0	Indicate that the operation is ended.

STATUS_EXCH (R)

Indicates on its most significant byte the error exchange status (bit set to 1). No error if this quartet is set to 0. The module resets this byte at each new command launched in EXE register (except S_TOC_EXE). The least significant byte indicates the smart card CRD flags and the FIFO state.

MOST SIGNIFICANT BYTE:

Bit	Name	Reset value	Function
b8	Bad_TS	0	Bad TS byte in ATR
b7	Bad_PB	0	Bad procedure Byte in T=0 exchange
b6	Err_Par	0	Parity error If character repetition option is disabled, a parity error on one byte has been detect. If character repetition option is enabled, the module ask three times the smart card to repeat. If the parity error is maintained, this status is returned.
b5	Err_EXE	0	A problem has occurred during the execution of EXE selected command. Check CRD flags.
b4	TOC	0	Timeout character
b3	TOB	0	Timeout block
b2	TOR	0	Timeout in Reset
b1	RFU	0	

LEAST SIGNIFICANT BYTE:

Bit	Name	Reset Value	Function
b8	CRD_INS	X	Presence Card Detector 0: No smart card 1: Smart card inserted
b7	CRD_ON	0	Smart card Vcc supply 0: Smart card has no Vcc 1: Smart card is powered
b6	CRD_ACT	0	Smart card reset indicator 0: Smart card has not been resetted 1: Smart card has been resetted
b5	CRD_SLEEP	0	Smart card sleep mode indicator 0: Smart card is in active mode (CLK active) 1: Smart card is in sleep mode (CLK at FRQ_MODE.CLK_LEV level)
b4	TR1	0	Data transmission mode on IO line (as specified in TS byte) 0: direct 1: inverse
b3	RFU	0	
b2	FIFO_FULL	0	FIFO full
b1	FIFO_EMPTY	1	FIFO empty

FIFO_FULL means that one or more bits of data have been overwritten. More than 261 bytes have been stored in FIFO. In this case the microprocessor must reset the FIFO because the data is corrupted.

FIFO_NB (R)

Indicates the number of bytes stored by the module in the FIFO. It is coded on two bytes (because FIFO is 261 bytes length). Its reset value is 0.

b8	b7	b6	b5	b4	b3	b2	b1	FIFO_NB
RFU	RFU	RFU	RFU	RFU	RFU	RFU	x	High order byte
x	x	x	x	x	x	x	x	Low order byte

IO_MUTE (R)

This register programs the watch dog on the IO line: each time the IO line goes low (at least once during character transmission for the start bit) the counter is reset, otherwise it is incremented at each etu.

It indicates the number of etus between two characters or more precisely the number of etus during which the IO line remains at level one. When the IO line falls to level zero, the counter is reset. Its reset value is 0.

b8	b7	b6	b5	b4	b3	b2	b1	IO_MUTE
x	x	x	x	x	x	x	x	High order byte
x	x	x	x	x	x	x	x	Low order byte

IO Registers

MANUAL_IN (R/W)

This register is used by the micro-controller to command smart card contacts.

Bit	Name	Reset value	Function
b8	Vcc_IN	0	Alim contact
b7	Vpp_IN	0	Vpp contact
b6	RST_IN	0	Reset contact
b5	CLK_IN	0	CLK contact
b4	I_O_IN	0	IO contact (bi-directional line)
b3	C4_IN	0	C4 contact (bi-directional line)
b2	C8_IN	0	C8 contact (bi-directional line)
b1	RFU	0	

***Note** : If AS/SY = 0 (asynchronous cards), CLK_IN is linked to the frequency generator, and if the MOTOROLA module is present, CLK_IN is bound to its ASYCLK pin.*

If AS/SY = 1 (synchronous cards), CLK_IN is controlled by the microprocessor, and if the MOTOROLA module is present, CLK_IN is bound to its SYNCLK pin.

MANUAL_OUT (R)

This register contains the smart card contacts values.

Bit	Name	Reset value	Function
b8	Vcc_OUT	0	Alim contact
b7	Vpp_OUT	0	Vpp contact
b6	RST_OUT	0	Reset contact
b5	CLK_OUT	0	CLK contact
b4	I_O_OUT	0	IO contact (bi-directional line)
b3	C4_OUT	0	C4 contact (bi-directional line)
b2	C8_OUT	0	C8 contact (bi-directional line)
b1	RFU	0	

***Note**: This register always represents the smart card's contact values, even if the MANUAL mode is disabled.*

After a soft reset of the module, the smart card contacts are deactivated.

FIFO_IN (W)

b8	b7	b6	b5	b4	b3	b2	b1	FIFO_IN
D8	D7	D6	D5	D4	D3	D2	D1	Data to store in FIFO (D8..D1)

***Note**: Writing data in the FIFO is forbidden if any of the following commands are running: PTS, EXCH, PON and RST.*

FIFO_OUT (R)

b8	b7	b6	b5	b4	b3	b2	b1	FIFO_OUT
D8	D7	D6	D5	D4	D3	D2	D1	Data to read in FIFO (D8..D1)

***Note**: In case of a soft reset of the module, this register will contain the FIFO's first byte that may have any value. The FIFO content is not set to 0 in the event of a soft reset.*

XOR_REG (R)

Contains the EXCLUSIVE OR (XOR) of the data stored in FIFO by the module. This register must be cleared before the first data concerned by this operation can be written in FIFO by the module.

b8	b7	b6	b5	b4	b3	b2	b1	XOR
D8	D7	D6	D5	D4	D3	D2	D1	Exclusive-or result (D8..D1)

b8	b7	b6	b5	b4	b3	b2	b1	Reset value
0	0	0	0	0	0	0	0	

CRC16 (R)

Contains the CRC16 calculation of the data stored in FIFO by the module. These registers must be cleared before the first data concerned by this operation can be written in FIFO by the module

b8	b7	b6	b5	b4	b3	b2	b1	CRC16
D8	D7	D6	D5	D4	D3	D2	D1	High order byte
D8	D7	D6	D5	D4	D3	D2	D1	Low order byte

b8	b7	b6	b5	b4	b3	b2	b1	Reset value
0	0	0	0	0	0	0	0	High order byte
0	0	0	0	0	0	0	0	Low order byte

MOTO_CFG (R/W)

This register enables the user to manually configure the device. The CARD_MODE.Moto_Sel bit must be set to 0.

Bit	Name	Reset value	Function
b8	RFU	0	
b7	RFU	0	
b6	RFU	0	
b5	RFU	0	
b4	VAL	0	Must be set to 1 during the manual configuration of the reader. Must be released to 0 after configuration.
b3	RDY	0	RDYMOD pin
b2	PWR	0	PWRON pin PWR = 0 : CRD_VCC = 3V PWR = 1 : CRD_VCC = 5V
b1	CSM	0	CS pin

The following sequence must be executed with at least two µs between each step:

VAL	RDY	PWR	CSM
1	0	X	1
1	0	X	0
1	0	X	1
1	1	1	0